SPECIFICATION

TO WHOM IT MAY CONCERN:

Be it known that we, with names, residence, and citizenship listed below, have invented the inventions described in the following specification entitled:

DRIVER-SIDE CURRENT CLAMPING WITH NON-PERSISTENT CHARGE BOOST

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DRIVER-SIDE CURRENT CLAMPING WITH NON-PERSISTENT CHARGE BOOST

Background of the Invention

[0001] When designing and manufacturing integrated circuits, it is often necessary to increase the speed at which signals propagate over a signal line. There are many ways of doing this. One way is to manipulate line-width and driver strength, including the use of tapered signal lines. Another way is to incorporate one or more repeaters (e.g., inverters) into a signal line. Yet other ways include custom design architectures and/or signal routes. These last options, however, are typically the most expensive (but sometimes necessary) way to speed signal propagation.

Summary of the Invention

[0002] One aspect of the invention is embodied in a method. In accordance with the method, a signal line is driven toward a first voltage by coupling a first current path to the signal line (under control of an input

signal). While the first current path is coupled to the signal line, 1) a non-persistent charge boost is provided to the signal line to increase the rate at which a voltage on the signal line switches toward the first voltage, and 2) current flow through the signal line is clamped to prevent the voltage on the signal line from reaching the first voltage.

[0003] Another aspect of the invention is embodied in a driver circuit. The driver circuit comprises a first current path that is coupled to a first voltage supply. A first switching circuit, under control of an input signal, couples and uncouples the first current path to an output of the driver circuit. A first current clamp, coupled in the first current path, prevents a voltage at the output from reaching the first voltage. A first non-persistent charge boost circuit, coupled to the first switching circuit, increases the rate at which the output switches toward the first voltage when the first current path is coupled to the output.

[0004] Other embodiments of the invention are also disclosed.

Brief Description of the Drawings

[0005] Illustrative and presently preferred embodiments of the invention are illustrated in the drawings, in which:

[0006] FIG. 1 illustrates a first exemplary method for increasing the

speed at which signals propagate over a signal line;

[0007] FIG. 2 illustrates a second exemplary method for increasing the speed at which signals propagate over a signal line;

[0008] FIG. 3 illustrates a first exemplary driver circuit that implements driver-side current clamping with a non-persistent charge boost;

[0009] FIG. 4 illustrates a second exemplary driver circuit that implements driver-side current clamping with a non-persistent charge boost;

[0010] FIG. 5 illustrates an exemplary timing of signals for the FIG. 4 driver circuit; and

[0011] FIG. 6 illustrates an alternate embodiment of the FIG. 4 driver circuit.

Description of the Preferred Embodiment

[0012] FIG. 1 illustrates a method 100 for increasing the speed at which signals propagate over a signal line. In accordance with the method, an input signal controls the coupling 102 of a first current path to a signal line. When the first current path is coupled to the signal line, 1) the signal line is driven toward a first voltage, 2) a non-persistent charge boost is provided 104 to the signal line to increase the rate at which a voltage on the signal line switches toward the first voltage, and 3) current flow through the signal line is clamped 106 to prevent the voltage on the signal line from reaching the first

voltage.

[0013] By providing the non-persistent charge boost to the signal line upon coupling the first current path to the signal line, the signal line is driven toward the first voltage more quickly, thereby increasing signal propagation speed over the signal line. By clamping current flow through the signal line and preventing the voltage on the signal line from reaching the first voltage, the degree to which voltage on the signal line needs to be swung to switch the signal line toward a second voltage is reduced, thereby increasing switching speed when the signal line needs to be driven toward the second voltage.

[0014] Although the method 100 may be used to increase signal propagation and switching speeds when only one current path is coupled and uncoupled from a signal line, it may be desirable to use the method 100 to increase signal propagation and switching speeds when coupling and uncoupling a pair of current paths to a signal line. Thus, for example, the method 100 may be extended as shown in FIG. 2.

[0015] The method 200 begins similarly to the method 100. However, the method 200 proceeds with the input signal changing state 202, thereby causing the first current path to be uncoupled from the signal line and causing a second current path to be coupled to the signal line. When the second current path is coupled to the signal line, 1) the signal line is driven toward a second voltage, 2) a non-persistent charge boost is provided 204 to the signal line to increase the rate at which the voltage on the signal line

switches toward the second voltage, and 3) current flow through the signal line is clamped 206 to prevent the voltage on the signal line from reaching the second voltage.

[0016] The methods 100 & 200 may be used in conjunction with methods that clamp the voltages allowed at a receiving end of a signal line to a range of voltages that is smaller than a range of voltages allowed at a driven end of the signal line. Such a voltage clamping method is taught in the United States patent number 6,351,171 of Balhiser entitled "Accelerated Interconnect Transmission via Voltage Clamping Toward Toggle Point" (which patent is hereby incorporated by reference for all that it discloses).

[0017] FIG. 3 illustrates a first embodiment of a driver circuit 300 that may be used to implement the method 100 or 200. The driver circuit 300 comprises a first current path 302 that is coupled to a first voltage (V1), and a second current path 304 that is coupled to a second voltage (V2). The driver circuit 300 further comprises a first switching means 306 to couple and uncouple the first current path 302 to an output of the driver circuit, and a second switching means 308 to alternately couple and uncouple the second current path 304 to the driver's output. A first current clamping means 310 is coupled in the first current path, and prevents a voltage at the driver output from reaching the first voltage. Likewise, a second current clamping means 312 is coupled in the second current path, and prevents the driver's output voltage from reaching the second voltage. When the first current path 302 is coupled to the driver output, a first non-persistent charge boost means 314,

coupled to the first switching means 306, increases the rate at which the driver's output voltage switches toward (but not to) the first voltage. Similarly, when the second current path 304 is coupled to the driver output, a second non-persistent charge boost means 316, coupled to the second switching means 308, increases the rate at which the driver's output voltage switches toward (but not to) the second voltage.

[0018] Note that although the driver circuit 300 comprises a current clamping means and non-persistent charge boost means coupled to each current path that influences the state of the driver's output, the driver circuit 300 could alternately comprise a current clamping means and/or non-persistent charge boost means coupled to only one of the current paths.

[0019] FIG. 4 illustrates a second embodiment of a driver circuit 400 that may be used to implement the method 100 or 200. The driver circuit 400 comprises first and second switching circuits 402, 404, each of which is controlled by an input signal received at node IN. By way of example, the switching circuits 402, 404 may form an inverting complimentary metal-oxide semiconductor (CMOS) buffer 406 (i.e., with the first switching circuit taking the form of a p-channel field effect transistor (PFET), and with the second switching circuit taking the form of an n-channel field effect transistor (NFET)). The PFET is coupled via its source and drain between an output of the driver circuit (NODE_0) and a first intermediate node (BNP_UP). The NFET is coupled via its source and drain between NODE_0 and a second intermediate node (BNP_DN). The gates of the two FETs are coupled to

each other at node IN, which is configured to receive an input signal.

[0020] The node BNP_UP is coupled to a first voltage (VDD) by means of a current clamp 408 and a non-persistent charge boost circuit 410. In a similar fashion, the node BNP_DN is coupled to a second voltage (GND) by means of a current clamp 412 and a non-persistent charge boost circuit 414. As shown in FIG. 4, corresponding ones of the clamps and boost circuits 408/410, 412/414 may be coupled in parallel, with each clamp taking the form of a resistor 416, 418, and with each boost circuit taking the form of a capacitor 420, 422.

[0021] In operation, a low input signal at node IN causes the PFET 402 to conduct, thereby causing a current path through PFET 402 and resistor 416 to be coupled to the driver's output (i.e., NODE_0). Assuming that capacitor 420 already holds a charge, the charge on the capacitor is now released to provide a non-persistent positive charge boost to the driver's output. This first non-persistent charge boost increases the rate at which the driver's output switches toward VDD. As the voltage on the driver's output rises, current flow at the output is impeded as a result of resistor 416, and the voltage at the driver's output is limited to something less than VDD. If the input signal then rises high, the PFET 402 will cease to conduct, and the NFET 404 will begin to conduct. Again, assuming that capacitor 422 already holds a charge, the charge on the capacitor is now released to provide a non-persistent negative charge boost to the driver's output. This second non-persistent charge boost increases the rate at which the driver's output

switches toward GND. As the voltage on the driver's output falls, current flow at the output is impeded as a result of resistor 418, and the voltage at the driver's output is limited to something more than GND.

[0022] When the current path through PFET 402 and resistor 416 is uncoupled from the driver's output, capacitor 420 is charged (or "armed") as a result of the voltage drop across resistor 416. Likewise, when the current path through NFET 404 and resistor 418 is uncoupled from the driver's output, capacitor 422 is charged as a result of the voltage drop across resistor 418. The implementation of the current clamps 408 and 412 therefore provides a means for arming the charge boost circuits 410 and 414.

[0023] As shown in FIG. 4, the output of the driver circuit 400 may be coupled to a signal line 424 that is associated with a line resistance (as illustrated by resistances R1 and R2) and a line capacitance (as illustrated by capacitances C1, C2 and C3). The receiving end of signal line 424 may be coupled to a receiver 426. By way of example, the receiver 426 is shown to be an inverting CMOS buffer. In such an arrangement, it may be beneficial to choose each of the charge boost capacitors 420, 422 such that its value is at least twice the sum of 1) the capacitance of the signal line 424, and 2) the gate capacitance of the receiver 426. Choosing larger values for the capacitors 420, 422 will provide more boost, but at the cost of more chip area; and choosing smaller values for the capacitors 420, 422 will diminish the boost. In choosing values for the clamping resistors 416, 418, it should

be noted that larger values decrease power consumption, but at the expense of greater chip area.

[0024] In accordance with the teachings of United States patent number 6,351,171, referenced supra, first and second voltage clamps 428, 430 may be coupled to the signal line 424 in proximity to the receiver 426. In this manner, the voltage at the receiver 426 may be prevented from reaching either of voltages VDD or GND. By way of example, each voltage clamp 428, 430 may be implemented by means of a series pair of diode-connected NFETs 432/434, 436/438. In one embodiment of the FIG. 4 apparatus, the range of voltages allowed at the driven end of the signal line 424 is smaller than the range of voltages between VDD and GND, but greater than the range of voltages allowed at the receiving end of the signal line. Thus, at any given instant, a voltage gradient exists on the signal line. In such an embodiment, the voltages appearing at nodes IN, BNP_UP, BNP_DN, NODE_0, NODE_99 and OUT as an input signal switches from GND to VDD and back to GND might appear as shown in FIG. 5.

[0025] FIG. 6 illustrates an alternate embodiment of the FIG. 4 driver circuit. In the driver circuit 600, additional non-persistent boost is provided by FETs 602, 606, each of which is coupled in parallel with a corresponding non-persistent charge boost capacitor 420, 422. Thus, as shown, NFET 602 may be coupled in parallel with capacitor 420, and PFET 606 may be coupled in parallel with capacitor 422 (with parallel connections being made with the source and drain terminals of each FET and its corresponding

capacitor). The gates of the FETs 602, 606 are coupled to the driver's output (i.e., NODE_0) via delay circuits 604, 608. In this manner, each FET conducts prior to when it is switched into the active current path of the driver circuit 600. In this manner, each FET brings its output node (BNP_UP or BNP_DN) to a maximum voltage (VDD or GND) prior to its output node being switched into the active current path of the driver circuit 600. However, as a result of the delay circuits 604, 608, the boost provided by each FET is non-persistent. For example, PFET 602 conducts while the gate of PFET 402 is driven high. When the gate of PFET 402 is driven low, PFET 602 provides a boost to NODE_0 until such time that the change of state of NODE_0 propagates through delay circuit 604 to thereby pull the gate of PFET 602 high and cause PFET 602 to cease conducting. At this point in time, clamp resistor 416 begins to limit the voltage at node BNP_UP. Later, when node BNP_UP is once again switched to the inactive current path of drive circuit 600, the existence of delay circuit 604 provides a period of time for clamp resistor 416 to charge boost capacitor 420 before PFET 602 once again begins to conduct.

[0026] Each of the delay circuits 604, 608 shown in FIG. 6 may be implemented using a chain of buffer or inverter elements. And, if separate control over the positive and negative charge boost delays is not needed, the delay circuits 604, 608 may be merged into a common delay circuit (not shown).

[0027] When used in conjunction with voltage clamping at the driven end

of a signal line, the methods and apparatus disclosed herein minimize the voltage gradient on a signal line and constrain the maximum and minimum charges stored on the signal line. This results in a lower RC time constant than using voltage clamping alone. It also results in less static current and, thus, less power dissipation. Two normally contradictory objectives may therefore be achieved. That is, static current is limited while dynamic switching current is virtually unimpeded (which typically results in power savings and faster signal propagation).

[0028] Of significance for some applications, the methods and apparatus disclosed herein may also be used as "in-place-optimizations" (IPOs) to fix problems with critical signal routes found late in the design and/or manufacture stage of an integrated circuit.

[0029] While illustrative and presently preferred embodiments of the invention have been described in detail herein, it is to be understood that the inventive concepts may be otherwise variously embodied and employed, and that the appended claims are intended to be construed to include such variations, except as limited by the prior art.